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RISC OS power on self test

RISC OS 3.10 performs a series of tests to the hardware of the system on power up. This Application note describes those tests and how to interpret the information provided by them.

Applicable Hardware :	Any ARM based system fitted with RISC OS 3.10.	Related Application Notes:	None

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In a normal power-on self test (POST) sequence, the screen colour is first set to purple to indicate testing has started. The first part of the test (which performs a brief ROM and RAM test and initialises the IO and Video controllers) passes within less than a second and is not easily visible. However, certain system failures may cause the machine to crash or halt during this phase : no further activity will occur and this may be read as a major failure, probably of the IO system.

The screen mode is set up to suit a simple 15kHz monitor (Monitor 0, Sync 0) and this will produce a signal unsuitable for VGA or High Resolution monitors, resulting in an unsynchronised screen display. If a stable display is not shown on a type 0 monitor, this may indicate either a video system fault or some more fundamental fault which stops the test software itself from running.

If the simple memory test referred to earlier is passed, a more extensive test occurs. During this phase - which is the longest part of the sequence, taking up to 12 seconds on a 16Mbyte machine - the screen colour is changed to blue. Again, the screen display will be unsynchronised on VGA or high resolution monitors.

After the main memory test, tests are performed on the video and sound controller, VIDC. These are again very brief.

Finally, the screen colour reverts to purple and a test is performed for an ARM 3 processor. This test relies on good RAM, and will not be performed if a failure has already been detected. However, an unexpected failure could leave a purple screen displayed, indicating a major system fault.

At the close of the test sequence, the screen colour is set to red if a failure has been recorded in the tests. A green screen will be shown if no faults are detected.

The self-test is now complete, and the system will normally start RISC OS. This is indicated by a black screen with a memory size message displayed. Note that the various power-on key combinations should be held until this message (or the red screen border resulting from a 'power-on delete' operation) appear; the keys will be ignored if released before the self-test sequence has completed.

If a fault has been detected, RISC OS will not immediately be started. Instead, the entire screen will change to red and the LED on the floppy disc drive will flash. The flashing sequence indicates the fault detected in accordance with the fault codes described later. An 8 digit hexadecimal number is displayed as 8 groups of 4 flashes, where a long flash indicates binary '1' and a short flash indicates binary '0'. Thus a ROM failure (fault code 00000219 on an ARM 3 machine) will be displayed as :

```
short short short short        0 (binary 0 0 0 0 0 0 0 0)
short short short short        0 (binary 0 0 0 0 0 0 0 0)
short short short short        0 (binary 0 0 0 0 0 0 0 0)
short short short short        0 (binary 0 0 0 0 0 0 0 0)
short short short short        0 (binary 0 0 0 0 0 0 0 0)
short short long  short        2 (binary 0 0 0 0 0 0 1 0)
short short short long         1 (binary 0 0 0 0 0 0 0 1)
long  short short long         9 (binary 0 0 0 0 1 0 0 1)
```

A CMOS RAM failure (fault code 00010000) will be displayed as:

```
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short long          0 (binary 0 0 0 0 0 0 0 1)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
short short short short         0 (binary 0 0 0 0 0 0 0 0)
```

Converting the binary into the hexadecimal number is a straight forward process if you are used to binary however if you are not used to using binary then it is best to write out a table and write out the binary numbers against it. The following table is for fault code 00000219.

```
128  64  32  16  8   4   2   1    Total
 0   0   0   0   0   0   0   0      0
 0   0   0   0   0   0   0   0      0
 0   0   0   0   0   0   0   0      0
 0   0   0   0   0   0   0   0      0
 0   0   0   0   0   0   0   0      0
 0   0   0   0   0   0   1   0      2  (a single 2)
 0   0   0   0   0   0   0   1      1  (a single 1)
 0   0   0   0   1   0   0   1      9  (add the 8 and the 1 to make 9)
```

If a POST interface box is connected, an overall PASS/FAIL message is displayed on the LCD with the same result code this will be either

```
        PASS :  xxxxxxxx
or      FAIL :  xxxxxxxx
```

where xxxxxxxx is a bitmap summarising the test results and other flags. The meaning assigned to these bits is as follows :

Status bits

```
   00000001        Self-test due to power-on
   00000002        Self-test due to interface hardware
   00000004        Self-test due to test link
   00000008        Long memory test performed
   00000010        ARM 3 fitted
   00000020        Long memory test disabled
   00000040        PC-style IO world detected
```

Fault bits

```
   00000200        ROM failed checksum test
   00000400        MEMC CAM mapping failed
   00000800        MEMC protection failed
 * 00001000        IOC register test failed
   00004000        VIDC (Virq interrupt) timing failed
   00008000        Sound (Sirq interrupt) timing failed
```

```
* 00010000        CMOS RAM (clock/calendar chip) unreadable
  00020000        Ram control line failure
  00040000        Long RAM test failure
```

Only bits 8 to 31 indicate faults : any of the status bits 0 to 7 may be set with a green screen and the PASS message displayed. Bit patterns not defined above may be assigned to future versions of the test software.

Test result indicators marked '*' are only used in later versions (RISC OS 3 ROMs).

Note that optional video mode enhancers may (due to fault or lack of software switching) power up in a mode that provides other than 24MHz to VIDC. This will result in Sirq and Virq failures (code 0000C00xx) being reported.

In order to avoid this problem, late versions of the POST (version 1.45, in RISC OS version 3.10) will disable the VIDC tests (as well as the long memory test) if bit 7 of byte &BC in CMOS RAM is set. On earlier POST versions (1.43, RISC OS 3.00) this bit will disable only the long memory test. This may be useful to owners of VGA/SVGA monitors which are unsynchronised for several seconds at boot time.

Additionally there is a piece of hardware called the POST (Power On Self Test) interface test box. The POST interface connect to any piece of equipment produced from the A540 onwards and provides meaningful messages on a display on the POST interface box.

The POST interface test box is available from Atomwide for £299.00 + VAT. Further details can be obtained from Atomwide directly.

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