Support Group Application Note
Number: 035
Issue: 1
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BBC Master 128
Cartridge Interface

This application note details the Cartridge Interface on the Master Series machines with differences for operation with the Electron Plus 1 noted where relevant.

Applicable Hardware : BBC Master 128

Related Application Notes:

Support Group
Acorn Computers Limited
Acorn House
Vision Park
Histon
Cambridge CB4 4AE

Abbreviations

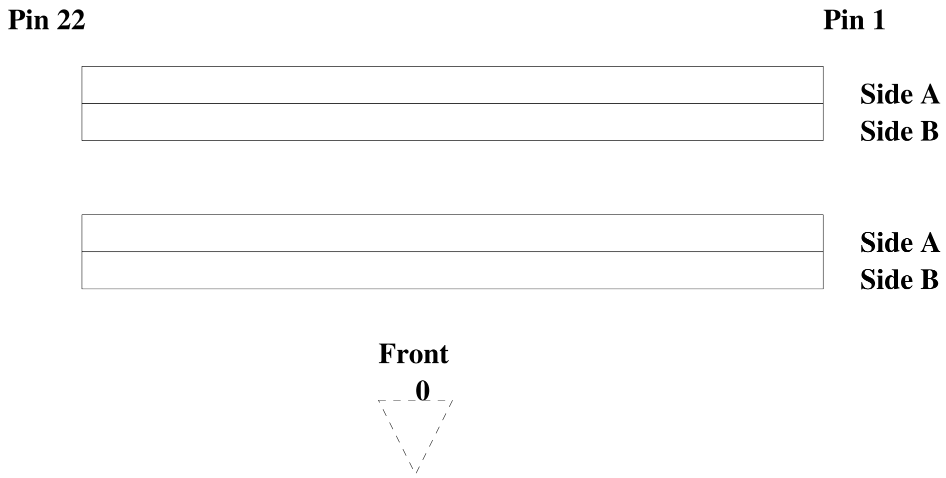
Abbreviations are used in this Note as follows:

A/L	Active Low
O/C	Open Collector output
CMOS	Complementary-symmetry Metal Oxide Semiconductor
CPU	Central Processor Unit ie, the microprocessor
TTL	Transistor-Transistor Logic
&	A hexadecimal number follows
n	As a signal prefix means Active Low output (A/L)
PCB	Printed Circuit Board
NMOS	Nitride-layer Metal Oxide Semiconductor

Cartridge Orientation

The cartridge pinning in the Master Series machine is arranged as follows:

Viewed from above



Components are normally mounted onto Side A of the PCB within the cartridge.

Pinout

Pins are described viewed from "within" the cartridge ie, an "Input" is an input to the cartridge. An "output" is an output to the computer.

SIDE A

1 +5V - Logic power supply.
150mA max in a Master with co-processor fitted and with disk drives.
50mA max in an Electron Plus 1.

2 nOE - Output Enable. Input from A/L CMOS level.
Low during PH12 period of system clock. It is intended to switch on the output buffers of cartridge memory devices. It is not guaranteed low at other times.

3	nRST - System Reset. Low during a system reset. It is not synchronised to any clock.	Input from A/L CMOS level.
4	CSRW - Chip Select - Read/Write. <u>Master</u> - Changes function according to the memory region that the CPU is addressing. During accesses to &FC00 through &FEFF it is equivalent to the CPU Read/Write line during nPH12. For all other accesses it is an Active High chip select for memory devices. It is not guaranteed low at other times. <u>Electron</u> - CPU Read/Write line.	Input from CMOS level.
5	A8 - Address line 8.	Input from TTL level.
6	A13 - Address line 13	Input from TTL level.
7	A12 - Address line 12	Input from TTL level.
8	PH12 - CPU clock. Computer's PH12 output.	Input from CMOS levels.
9	-5V - Negative supply voltage. 20mA max. This -5V may not be available on all Acorn Cartridge Interfaces. To ensure compatibility, negative voltages should be generated within the Cartridge if required.	
10	CSYNC/MADET <u>Master</u> - There are two functions dependent upon link 12 in the computer: E/nB - the default function. It enables cartridges to know which machine they are plugged into. It is connected to 0V in the Master (and unconnected in the Electron). Link 12 is set to position B. CSYNC - Composite Sync. System Vertical & Horizontal sync is made available fro Genlock use. Set Link 12 to position B. <u>Electron</u> - Unconnected.	 Input from TTL levels.
11	RNW/READY <u>Master</u> - R/W - Data Direction Control. System data buffer direction control. If low, cartridges are being written to; if high and selected, they may drive the bus during PH12. <u>Electron</u> - READY - CPU wait state control When driven low, this line will cause the CPU to extend it's cycle until READY is released. Only works with CMOS CPUs. Will only work on READ cycles with NMOS CPUs.	 Input from TTL levels O/C A/L output
12	nNMI - Non-maskable Interrupt. Connected to the system NMI line.	O/C A/L output.
13	nIRQ - Interrupt request. Connected to the system IRQ line.	O/C A/L output.

14 nINFC - Internal Page &FC Input from TTL levels. A/L.
Memory Active decode input.
<u>Master</u> - When bit IFJ in the Master ACCON register (via &FE34) is set, all accesses to &FC00 through &FCFF will cause this select to become active.
<u>Electron</u> - Not applicable.

15 nINFD - Internal Page &FD Input from TTL levels. A/L.
Memory Active decode input.
<u>Master</u> - When bit IFJ in the Master ACCON register (via &FE34) is set, all accesses to &FD00 through &FDFF will cause this select to become active.
<u>Electron</u> - Not applicable.

16 ROMQA - Memory paging select Input from TTL levels.
This is the least significant bit of the ROM select latch located at &FE30 in the Master, and at &FE05 in the Electron.

17 Clock Input/Output TTL levels.
<u>Master</u> - Links on the computer select one of two functions:
a) 16Mhz Output to computer (Link DB only).
b) 8 Mhz Input to cartridge (Link CD in addition to AB).
The user should ensure that the links are set correctly, and that there is proper termination. Normally only AB is linked in the computer.
WARNING! If Link AB in the computer is removed, the dynamic RAM could be damaged unless a clock supply is fed into the computer AT ALL TIMES whilst the computer is powered. The user must ensure that the Cartridge cannot be removed by accident and interrupt the clock supply. The use of this clock facility must be at the users risk.
<u>Electron</u> - 16 Mhz input.

18 nROMSTB/nCRTCRST TTL levels.
<u>Master</u> - nCRTCRST is an Active Low Output signal of the system CRTC reset input. It is provided for Genlock use.
<u>Electron</u> - nROMSTB is an Active Low Input which selects &FC73. It is intended to be used as a Paging Register.

19 ADOUT - System audio output.
Filtered output of the sum of all audio inputs to the computer. No significant load should be taken from this pin.

20 AGND - Audio Ground.
The zero volt return for ADOUT. It should be used instead of system 0V to minimise audio noise.

21 ADIN - Cartridge audio input.
<u>Master</u> - An output to the computer's audio circuitry. It "sees" an impedance of at least 1K ohm. Only one cartridge using this output should be connected to the computer at one time.
<u>Electron</u> - This is a connection from one cartridge to another.

22 0V - Zero volts.
System earth return for digital signals.

SIDE B

1	+5V - Logic power supply. 150mA max in a Master with co-processor fitted and with disc drives. 10mA max in an Electron Plus 1.	
2	A10 - Address line 10.	Input from TTL levels.
3	D3 - Data bus line 3.	Input/Output TTL levels.
4	A11 - Address line 11.	Input from TTL levels.
5	A9 - Address line 9.	Input from TTL levels.
6	D7 - Data bus line 7.	Input/Output TTL levels.
7	D6 - Data bus line 6.	Input/Output TTL levels.
8	D5 - Data bus line 5.	Input/Output TTL levels.
9	D4 - Data bus line 4.	Input/Output TTL levels.
10	nOE2/LPSTB - O/P Enable/Light Pen Strobe. Master - With link 21 removed in the computer, this pin provides a connection between the two cartridges. With the link in place, the pin forms a connection to a pull-up resistor in the computer to +5V. The connection is also made to the CRTC Light-Pen Strobe and interrupt structure. Electron - This provides an additional A/L enable for ROMs in the Electron. This corresponds to ROM position 13 and responds quickly to Service Calls. It is low during the A/L portion of PH12. It is not guaranteed high at other times.	Input from TTL levels.
11	BA7 - Buffered address line 7. Master - This line holds addresses valid for 125nS after PH12 goes low. Electron - This is not buffered nor held valid for an extended period in the Electron.	Input from TTL levels.
12	BA6 - Buffered address line 6. see pin 11.	Input from TTL levels.
13	BA5 - Buffered address line 5. see pin 11.	Input from TTL levels.
14	BA4 - Buffered address line 4. see pin 11.	Input from TTL levels.
15	BA3 - Buffered address line 3. see pin 11.	Input from TTL levels.
16	BA2 - Buffered address line 2. see pin 11.	Input from TTL levels.
17	BA1 - Buffered address line 1. see pin 11.	Input from TTL levels.

18	BA0 - Buffered address line 0 see pin 11.	Input from TTL levels.
19	D0 - Data bus line 0.	Input/Output TTL levels.
20	D2 - Data bus line 2.	Input/Output TTL levels.
21	D1 - Data bus line 1.	Input/Output TTL levels.
22	0V - Zero volts. Digital signal Earth return.	