Support Group Application Note
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Author:

Acorn Electron Expansion Application Note

The information contained in this application note is provided as a guide to developers of expansion modules for the Acorn Electron.

Applicable Hardware : Acorn Electron

Related Application Notes:

Support Group
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1.0 Purpose of this application note

1 To describe the signals available on the expansion port at the rear of the Electron microcomputer.

2 To define the specification which all expansion modules for the Electron microcomputer must meet.

3 To describe Acorn Computers' philosophy for expansion of the Electron microcomputer.

Note that both hardware and software must conform to the standards set out in this note. Failure to do this will result in poor reliability, and incompatibility with other expansion modules and the Electron itself. Failure to comply with the power supply requirements may cause the thermal fuse in the mains power adaptor to blow irretrievably.

1.1 Acorn Expansion Module Philosophy

The Electron is designed to take one or two expansion units fixed rigidly to the main unit and to one another by screws which locate into recessed brass bosses. More expansion units can be added with consequent loss of rigidity.

Electrical connection is to the PCB edge connector at the back of the Electron. Dimensions and specifications for the expansion connector are given in section 2 and the Appendix.

2.0 Electron Expansion Connector

Pinout

To gain access to the Electron expansion connector, the plastic cover which protects it must be removed. Any instructions supplied with an expansion module must direct the user to remove this cover before attempting to connect the module to the Electron, and to replace the cover whenever the module is disconnected.

The Electron expansion connector is laid out as shown in Figure 1.

Bottom			**Top**
18V AC	**2**	**1**	**18V AC**
AC RETURN	**4**	**3**	**AC RETURN**
-5V	**6**	**5**	**-5V**
0V	**8**	**7**	**0V**
+5V	**10**	**9**	**+5V**
16MHz	**12**	**11**	**SOUND O/P**
PHI OUT	**14**	**13**	**÷ 13 IN**
$\overline{\mathbf{NMI}}$	**16**	**15**	$\overline{\mathbf{RST}}$
$\mathbf{R/\overline{W}}$	**18**	**17**	$\overline{\mathbf{IRQ}}$
D6	**20**	**19**	**D7**
D4	**22**	**21**	**D5**
D2	**24**	**23**	**D3**
D0	**26**	**25**	**D1**
NC	**28**	**27**	$\overline{\mathbf{RDY}}$
SLOT	**30**	**29**	**SLOT**
A14	**32**	**31**	**A15**
A12	**34**	**33**	**A13**
A10	**36**	**35**	**A11**
A0	**38**	**37**	**A9**
A2	**40**	**39**	**A1**
A4	**42**	**41**	**A3**
A6	**44**	**43**	**A5**
A8	**46**	**45**	**A7**
0V	**48**	**47**	**0V**
+5V	**50**	**49**	**+5V**

Figure 1 : Layout of Electron Expansion Connector

2.1 Signal Definitions

The function of each terminal on the Electron expansion connector is described below.

18V AC (pins 1,2)
AC RETURNS (pins 3,4)
These lines are connected directly to the output from the Electron mains power adaptor. A total of 6W may be drawn from these lines as long as no power is taken from +5V (pins 9,10,49,50). For safety reasons these lines must never be used as an AC input to the Electron, see Section 3.

-5V (pins 5,6)	A -5V supply from the Electron. Up to 20mA (total) may safely be drawn from this line by expansion modules.
0V (pins 7,8,47,48)	Ground. Expansion modules with their own power supply must have the 0V lines commoned with the Electron.
+5V (pins 9,10,49,50)	A +5V supply from the Electron. Up to 500mA (total) may safely be drawn from this line by expansion modules as long as no power is taken from 18V AC (pins 1,2,3,4).
SOUND O/P (pin 11)	Sound output. A 3V peak to peak source via a 1K series resistor from the Electron ULA.
16 MHz (pin 12)	16 Megahertz from the Electron main oscillator. This output may be used for clock generation within an expansion module.
/13 IN (pin 13)	16 Megahertz divided by 13. This output may be used for baud rate generation. If divided by 1024 it will give approximately 1200Hz.
PHI OUT (pin 14)	The 6502 input clock. The low time is nominally 250ns. The high time may be 250ns (2MHz operation when reading ROMs) or 750ns or 1250ns (stretched clock for a 1MHz access, the length depending on the phase of the 2MHz clock) or up to 40us (if in modes 0-3). For further details see Section 4.
RST (pin 15)	Reset (active low). This is an OUTPUT ONLY for the system reset line. It may be used to initialise expansion modules on power up and when the BREAK key is pressed.
NMI (pin 16)	Non-Maskable Interrupt (negative edge triggered). This is the system NMI line which is open collector (wire-OR) and may be asserted by an expansion module. The pull-up resistor on this line inside the ULA is 3k3. Care must be taken to avoid masking other interrupts by holding the line low. Using NMI on the Electron requires knowledge of operating system protocols.
IRQ (pin 17)	Interrupt Request (active low). This is the system IRQ line which is open collector (wire-OR) and may be asserted by an expansion module. The pull-up resistor on this line inside the ULA is 3k3. It is essential for the correct operation of the machine that interrupts to not occur until the software is capable of dealing with them. Interrupts on the Electron expansion bus should therefore be disabled on power-up and reset. Significant use of interrupt service time may affect other machine functions, eg the real time clock. For further details see Section 4.
R/W (pin 18)	The system read/write line from the 6502.
D7-D0 (pins 19-26)	Bi-directional data bus. The direction of data is determined by R/W.
RDY (pin 27)	6502 ready line (active low). May be asserted by an expansion module to stop the processor when reading slow memory. This line works on read only (R/W=1).

(pin 28)	No connection
(pins 29,30)	Polarising key connector.
A0-A15 (pins 31-46)	6502 address bus.

3.0 Power Supply

Electron power supply:

Note carefully: instructions supplied with any expansion unit must state that all power supplied to the Electron and the expansion unit must be turned off before the expansion module is connected to or disconnected from the Electron.

The Electron power supply may be used to power expansion modules to a total of 500mA drawn from the +5V terminal on the expansion connector, and 20mA from the -5V terminal. THESE ARE TOTAL FIGURES FOR ALL EXPANSION UNITS COMBINED.

The 18V AC terminals on the expansion connector may be used to drive a low voltage power supply in the expansion module, but the total power drawn from the Electron mains power adaptor must never exceed 14 watts (worst case). If no power is being drawn by the expansion unit from the Electron's +5V supply then 6W may safely be drawn from the 18V AC lines on the expansion connector. The thermal fuse in the mains power adaptor is blown irretrievably if these values are exceeded.

Expansion power supply:

To accommodate expansion modules and combinations of modules which require more current, a separate power supply must be used. When this is done, the 0V rail of the expansion module must be connected to the 0V terminal of the Electron expansion connector. The +5V rail and the -5V rail (if implemented) must remain isolated from the Electron.

On no account should an expansion module power supply be designated to drive the Electron's 18V AC lines. This could create a conflict with the Electron's own AC supply, and would be extremely dangerous if the Electron's mains power transformer were plugged into the Electron when disconnected from the mains.

4.0 Timing

Processor Clock:

The Electron clock changes speed depending on what is being accessed at the time.

During accesses to the ROM the processor runs at 2MHz; PHI OUT is low for 250ns followed by high for 250ns (nominal).

During access to I/O and to RAM in modes 4-6 the processor runs at 1 MHz. The transition from 2Mhz to 1MHz is accomplished by having PHI OUT low time of 250ns followed by a high time of either 750 or 1250ns depending on the phase of the 2MHz signal, see Figure 2. The reason for this is that the processor will re-synchronise to the 1Mhz clock, making interfacing to peripherals such as the 6522 possible. The

1MHz clock is not available outside the ULA; it must be generated externally.

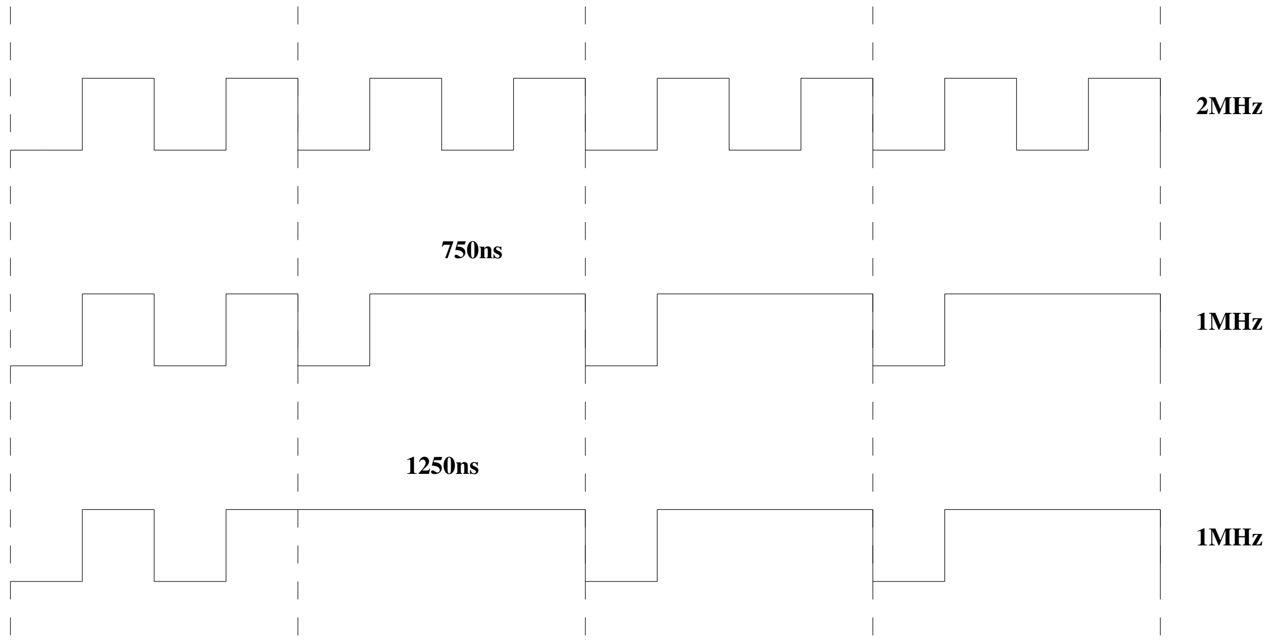

Figure 2 : Transition from 2MHz to 1MHz

In modes 0-3 the processor is denied access to the RAM during the displayed portion of the screen (40us out of 64us in 256 lines out of 312). If the processor requires access to the RAM during this time it is forced to wait until the end of the 40us line display period. ROM access during this time is allowed. The effect of all this is that the processor clock may be stretched in the high state for a period of up to 40us.

4.1 Regeneration of PHI

The timing of signal supplied to the Electron expansion are 16MHz, PHI OUT (the processor input clock), and 16M/13 (for baud rate generation). Signals such as 1MHz and 2MHz are used inside the ULA but do not exist outside. Since, for example, the 6522 needs a 1MHz clock in phase with the processor clock, this must be generated externally, see Figure 3.

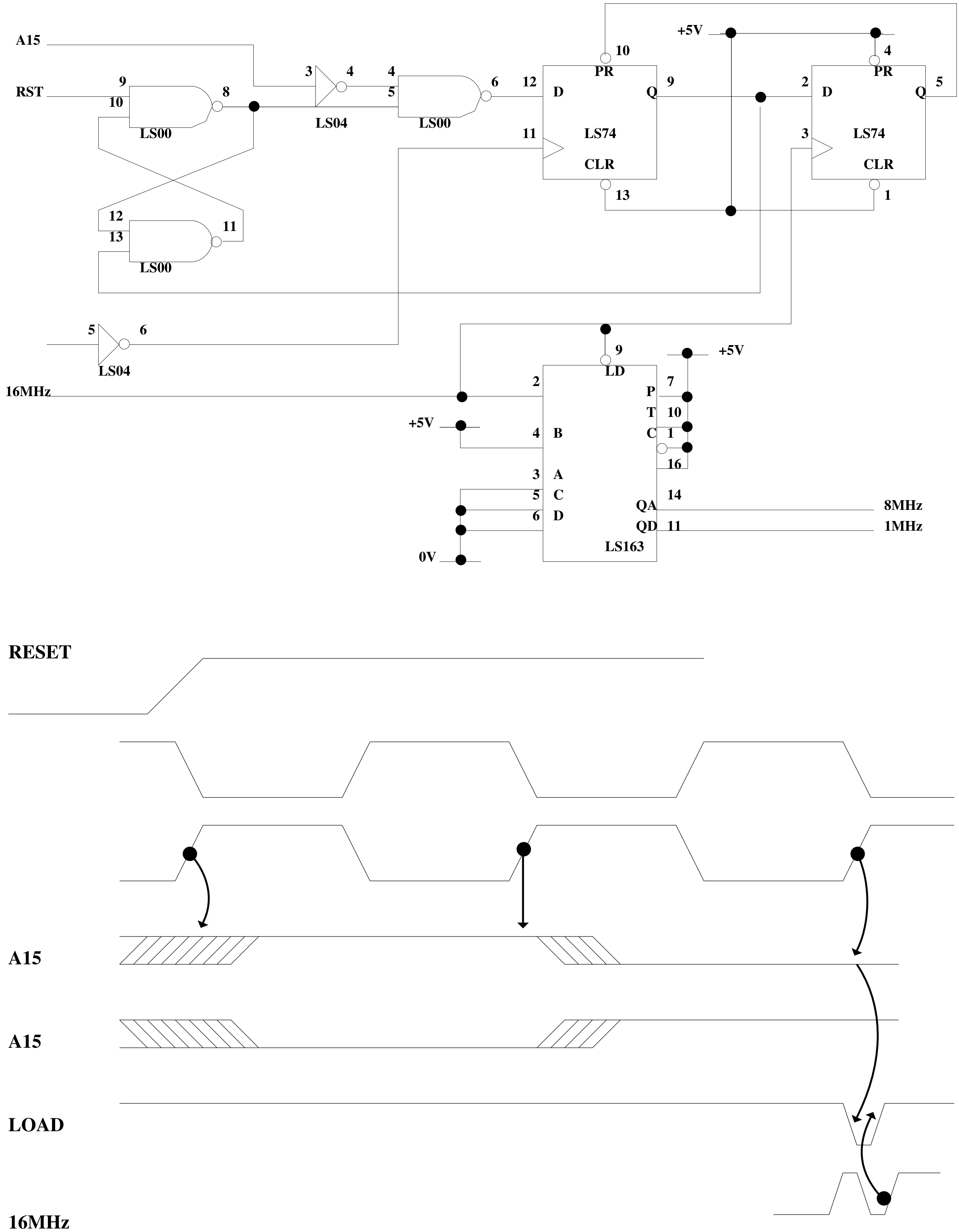

Figure 3 : 1MHz Regeneration Circuit

4.2 Interrupt Latency

The longest period for which interrupts (IRQs) are disabled determines the frequency at which new interrupts can be serviced. When the Electron is in modes 0-3 this period (known as interrupt latency) can be as long as 10ms worst case. This can cause problems for RS423, A/D conversion, etc.

In modes 4-6 the interrupt latency is 4ms worst case, so actions which require fast access or high data rate must force the Electron into one of these modes.

Use of an ACIA or UART with FIFO capability and/or a handshake will increase data throughput.

5.0 Sideways ROMs

Decoding:

Decoding of sideways ROMs is carried out at location &FE05. Any expansion module which uses sideways ROMs must include circuitry to intercept the write to &FE05 and act appropriately. The ULA handles the keyboard (ROM numbers 8 and 9) and BASIC (ROM numbers 10 and 11). These four ROM numbers are decoded inside the Electron itself and are not available for use by an expansion module. All other ROM calls must be decoded by the expansion module at address &FE05.

Twelve sideways ROMs can be accommodated on the Electron expansion, and four (ROM numbers 12 to 15) are accessible by a single write to &FE05.

	D7	D6	D5	D4	D3	D2	D1	D0
Write at &FE05	0	0	0	0	1	1	R1	R0

Where R1 R0 selects which of the four ROMs is required. These four ROMs are numbered 12 to 15.

Selection of a ROM number 12 to 13 will take the following form:

```
LDA#   ROMnumber
STA    &F4
STA    &Fe05
```

The write to &F4 must be carried out before the write to &FE05 in case an interrupt occurs. The write to &FE05 tells the ULA that a sideways ROM is to be accessed and it passes control to the operating system. Hardware in the expansion module must decode the write to &FE05 and select one of the four ROMs.

Now that BASIC has been de-selected, a further write to &FE05 can be decoded by the expansion module to select ROMs numbered from 0 to 7.

	D7	D6	D5	D4	D3	D2	D1	D0
Write at &FE05	0	0	0	0	0	R2	R1	R0

where R2 R1 R0 select which of the eight ROMs is required. These eight ROMs are numbered 0 to 7.

Once again, the write to &FE05 must be decoded by hardware in the expansion module which selects one of the eight ROMs.

Selection of a ROM number 0 to 7 will take the following form:

```
LDA#   &0C     \to
STA    &F4     \deselect
STA    &FE05  \BASIC
LDA#   ROMnumber
STA    &F4
STA    &FE05
```

On power-up, sideways ROMs are polled in the order 15 through to 0 to find the first which is configured as a language ROM. Execution will then commence in this ROM. As BASIC is ROM number 10/11, a ROM in an expansion module which is required to power-up before BASIC must be numbered 12 to 15.

ROM number allocation:

ROM selected by one write to address &FE05 are numbered 12 to 15, specified by 1100, 1101, 1110, 1111 in D3 D2 D1 D0 respectively. These ROMs are allocated to high priority NMI devices, or language which is to boot up before BASIC (eg a games cartridge).

ROMs selected by two writes to address &FE05 are numbered 0 to 7, specified by 0000, 0001, 0010, 0100, 0101, 0110, 0111 in D3 D2 D1 D0 respectively. These ROMs are low priority.

Acorn Plus 1 priority is forced as follows, highest priority first:

15 to 12
7 to 0
BASIC

This means that if sideways ROMs are used with the Plus 1 fitted then a language in 0 to 7 will power-up ahead of BASIC.

ROM number allocation is as follows:

0,1	Second external socket on expansion module (SK2)
2,3	First external socket on expansion module (SK1)
4-6	User applications
7	Modem
8,9	Keyboard
10,11	BASIC
12	Expansion module operating system
13	High priority slot in expansion module
14	ECONET
15	Disc

6.0 Mechanical Constraints

Expansion modules must be designed to mate mechanically with the rear of the Electron (relevant dimensions are given in the Appendix). Note that the case of any expansion module should have a protruding tongue which locates, with the clearance shown, into the cutout at the rear of the Electron. This ensures that the connector cannot be inserted crookedly. A simple connector without case location is not sufficient: if the connect is inserted crookedly while the power is on (in such a way as to short adjacent tracks), damage can be done to the Electron. For secure attachment, modules should be supplied with captive screws which locate into recessed brass bosses at the rear of the Electron.

7.0 Compatibility with Acorn Expansion Modules

I/O space

Page &FC in memory is reserved for peripherals with small memory requirements. Only one peripheral will be allocated to each group of addresses. Use of any memory areas not designated for user applications may lead to conflict with expansion modules produced by Acorn.

Initial allocations of space are as follows:

FC00 to FC0F	Test hardware
FC10 to FC13	TELETEXT
FC14 to FC1F	PRESTEL
FC20 to FC27	IEEE 488 Interface
FC28 to FC2F	ECONET
FC30 to FC3F	CAMBRIDGE RING interface
FC40 to FC37	WINCHESTER disc interface
FC48 to FC5F	Reserved for ACORN expansions
FC60 to FC6F	ACIA
FC70	A to D conversion
FC71	CENTRONICS
FC72	Status register - BSY ADC FB2 FB1 x x x x FB1 - fire button 1 FB2 - fire button 2 ADC - end of A to D conversion BSY - printer busy x - undefined
FC73	Sideways scrolled ROM control register
FC74 to FC7F	Reserved for ACORN expansions
FC80 to FC8F	Test hardware
FC90 to FC9F	Sound/speech
FCA0 to FCAF	Reserved for ACORN expansions
FCB0 to FCBF	VIA/real-time clock
FCD0 to FCDF	Floppy disc controller
FCE0 to FCEF	THE TUBE
FCF0 to FCFE	User applications
FCFF	Paging register for JIM

ROM numbers:

Use of sideways ROM numbers other than those designated for user applications may cause conflict with expansion modules produced by Acorn. Connection of two expansion modules which use the same ROM number will cause the system to crash and may result in damage to the expansion units or to the Electron.

7.1 BS 415

Any expansion module must meet BS 415 Class 1 specification for electrical safety.

7,2 Electron expansion middle module data buffer control

As two expansion modules can be used on the Electron simultaneously and in any order, there may be a conflict on the data bus during read cycles if buffers in a rear expansion unit are enabled when a peripheral device in a middle expansion unit is being accessed. Also, data buffers in expansion units must never be enabled when the Electron's own internal ROMs (8 to 11) are being accessed.

To prevent these collisions, a buffer enable line has been allocated through which an expansion module will enable the data buffers of the expansion module behind it when required. As Acorn have allocated the spare pin on the expansion connector (pin 28) to SOUND IN, pin 27 (the RDY line on the expansion connector) has been chosen to fulfil this buffer enable function in middle expansion modules.

Further details of the requirements and procedures for gaining approval should be obtained from Acorn Computers Limited.

APPENDIX

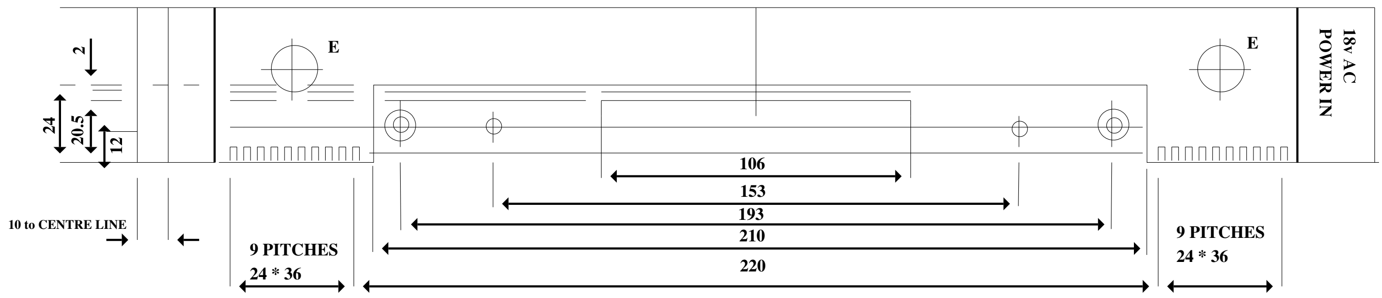

Figure 5 : Case dimensions around Electron expansion connector

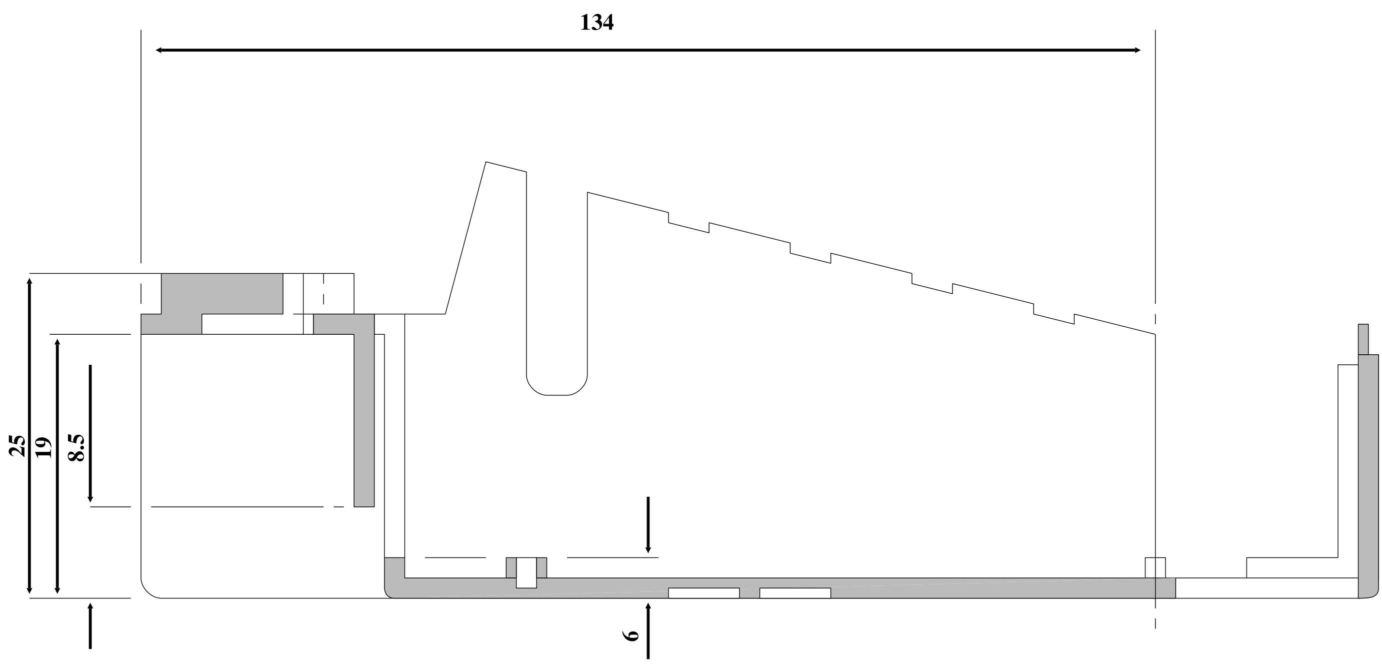

Figure 6 : Fixing hole gauge M6