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Acorn Electron Cartridge Interface Specification

This specification details the characteristics of the Cartridge interface as fitted to the Acorn Electron and BBC Master 128 computers.

The specification details the physical and electrical characteristics and software environment of the cartridges.

Applicable Hardware : Acorn Electron

Related Application Notes:

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1.0 Terminology

CMOS - Complementary metal-oxide-silicon technology

CPU - The microprocessor in the host computer

TTL - Transistor/Transistor Logic

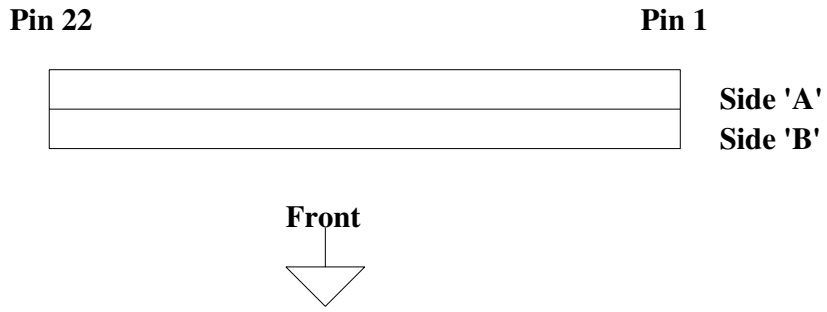
& - As a number prefix means a hexadecimal number follows

n - As a signal prefix means the signal is active low

2.1 Host Computer Connection

Cartridges plug into a 44 way gold plated edge connector arranged on each side of a 0.05 inch slot as 22 ways of 0.05" x 0.5" on 0.1" centres. The connectors are parallel to the front of the computer with the front and rear facing sides designated 'B' and 'A' respectively. Pin 1 of each side is on the far right. This is shown below:

Viewed From Above



Cartridges are aligned and polarised by the case; they are plugged vertically into the host. All cartridges constructed to the time of writing have the components mounted on the pcb 'A' side.

2.2 Pinout

The pins are described as seen from the cartridges; ie an input to the cartridge.

SIDE 'A'

1 +5V - Power supply
This is the system logic supply rail. No more than 150mA should be drawn by a cartridge in a fully configured Master 128 computer, ie with internal co-processor fitted. No more than 50mA should be drawn by a cartridge fitted to the Electron.

2 n0E - Output Enable : Input with CMOS levels
This is an active low signal during the PH12 period of the system clock. It is intended to switch on the output buffers of memory devices in cartridges. It is not guaranteed to be high at other times.

The front cartridge slot is allocated to system ROM positions 0 and 1. The rear slot is allocated to positions 2 and 3.

3 nRST - System Reset : Input with CMOS levels
This signal is active low during system reset. It is not synchronised to any internal clock.

4 CSRW - Chip Select / Read/Write : Input with CMOS levels
On the Electron:
This pin is the CPU read/write line.

On the Master 128:
This pin changes function according to the memory region that the CPU is addressing. During accesses to devices in the region &FC00 to &FEFF it is equivalent to the CPU read/write line during nPH12. For all other accesses it is an active high chip select for memory devices. It is not guaranteed to be low at other times.

This approach is necessary for compatibility with the Electron.

5 A8 - Address line 8 : Input with TTL levels

6 A13 - Address line 13 : Input with TTL levels

7 A12 - Address line 12 : Input with TTL levels

8 PH12 - CPU clock : Input with CMOS levels
This input is the host computer PH12out.

9 -5V - The negative supply voltage
No more than 20mA per cartridge should be drawn from this supply.

10 CSYNC/MADET
On the Electron:
This is a "no connect" on the Electron.

On the Master 128:
This pin has two functions dependant on the position of a link in the host computer:-

E/nB: this is the default function. It allows hardware in cartridges to "know" which into which type of computer it is plugged. It is a direct connection to+0V in the Master 128 and a floating node in the Electron.

CSYNC - Composite Synchronisation: Input with TTL levels
The system composite vertical and horizontal synchronisation is made available. It is intended to be used in genlock applications.

11 RNW/READY
This has different functions on the Electron and the Master 128.

On the Electron:
READY - CPU wait state control : Open collector output
When driven low, this line will cause the CPU to extend its cycle until READY is released. This will

only work on Electrons with CMOS CPUs. With NMOS CPUs it will only work on read cycles.

On the Master 128:
R/W - Data Direction Control : Input with TTL levels
This is the system data buffer direction control. If low, cartridges are being written to; if high and selected they may drive the bus during PH12.

12 nNMI - Non maskable interrupt : Open collector output
This signal is connected to the system NMI line. It is active low.

13 nIRQ - Interrupt request : Open collector output
This signal is connected to the system IRQ line. It is active low.

14 nINFC - Internal Page &FC : Memory active decode input : TTL active low
When bit IFJ is set in the Master 128 ACCCON register, all accesses to the address range &FC00 to &FCFF will cause this select to become active. The ACCCON access is not applicable to the Electron.

15 nINFD - Internal page &FD : Memory active decode input : TTL active low
When bit IFJ is set in the Master 128 ACCCON register, all accesses to the address range &FD00 to &FDFF will cause this select to become active. The ACCCON access is not applicable to the Electron.

16 ROMQA - Memory paging select : Input with TTL levels
This is the least significant bit of the ROM select latch located at &FE30 in the Master 128 and at &FE05 in the Electron.

17 Clock
This connection has different uses in the Electron and Master 128:

In the Electron:
Clock is a 16MHz input with TTL levels.

In the Master 128:
Clock is a strap selectable function:
a) 16MHz input with TTL levels.
b) 8 MHz input with TTL levels.
The functions are selected by links on the host computer. The user should ensure that the links are correct for a given application and that proper termination is provided.

18 nROMSTB/nCRTCRST
This has different functions on the Electron and Master 128:

On the Electron:
nROMSTB is an active low input using TTL levels which selects the location &FC73. This is intended to be used as a paging register.

On the Master 128:
nCRTCRST is an active low output signal meeting TTL levels of the system CRTC reset input. It is provided for use in genlock applications.

19 ADOUT - System audio output
This is the filtered output of the sum of all audio inputs to the host computer. No significant load should be taken from this node.

20 AGND - Audio Ground
This is the zero volt return for ADOUT. It should be used instead of the system zero volt connection to reduce audio noise.

21 ADIN - Cartridge audio output
In the Electron:
This is merely a connection from one cartridge to the other.

In the Master 128:
This is an output to the host computer audio circuitry. It 'sees' an impedance of at least 1.0kOhms. Two cartridges with audio output should not be inserted into the host computer at the same time.

22 0V - Zero volts
This is the system earth return for digital signals.

SIDE 'B'

1 +5V - Power supply
This is the system logic supply rail. No more than 150mA should be drawn by a cartridge in a fully configured Master 128 computer, ie with internal Second Processor fitted. No more than 10mA should be drawn by a cartridge fitted to the Electron.

2 A10 - Address line 10 : Input with TTL levels

3 D3 - Data bus line 3 : Input/Output with TTL levels

4 A11 - Address line 11 : Input with TTL levels

5 A9 - Address line 9 : Input with TTL levels

6 D7 - Most significant data bus line : Input/Output with TTL levels

7 D6 - Data bus line 6 : Input/Output with TTL levels

8 D5 - Data bus line 5 : Input/Output with TTL levels

9 D4 - Data bus line 4 : Input/Output with TTL levels

10 nOE2 - Output Enable : Input with TTL levels
This line provides an additional active low output enable for ROMs in the Electron. This corresponds to ROM position 13 and consequently responds quickly to service calls. it is low during the active low portion of PH12. It is not guaranteed to be high at other times.

LPSTB - Light pen strobe
A connection with a pull up to +5V is provided to the CRTC light pen strobe and system interrupt structure. When an on-board link is removed, this connection is merely a link from one cartridge to the other.

11 BA7 - Buffered address line 7 : Input with TTL levels
The buffered address lines hold addresses valid for 125ns after PH12 goes low. They are not buffered or held valid for an extended period in the Electron.

12 BA6 - Buffered address line 6 : Input with TTL levels

13 BA5 - Buffered address line 5 : Input with TTL levels

14 BA4 - Buffered address line 4 : Input with TTL levels

15 BA3 - Buffered address line 3 : Input with TTL levels

16 BA2 - Buffered address line 2 : Input with TTL levels

17 BA1 - Buffered address line 1 : Input with TTL levels

18 BA0 - Buffered address line 0 : Input with TTL levels

19 D0 - Data bus line 0 : Input/Output with TTL levels

20 D2 - Data bus line 2 : Input/Output with TTL levels

21 D1 - Data bus line 1 : Input/Output with TTL levels

22 0V - Zero volts
This is the earth return for digital signals

Where two or more cartridges are fitted, any host computer links affect ALL cartridges.

3.0 Memory Map

All accesses to the cartridges are performed at 2MHz. The memory map within the area &FC00 to &FD00 differs between the Electron and the Master 128:

3.1 Master 128 Memory Map

At the time of writing the memory map within the areas INFC and INFD in the Master 128 computer are as follows:

&FCFF	Paging register for memory in the &8000 to &BFFF region. Paging logic has to be implemented in each cartridge as necessary.
&FC82	
&FC81	Speech system

&FC80 to &FCFE	Reserved for use by Acorn.

3.2 Electron Memory Map

&FC18 to &FC1F	Reserved for use by Acorn
&FC28 to &FC2F	Reserved for Econet use
&FC30 to &FC3F	Reserved for use by Acorn
&FC60 to &FC6F	ACIA
&FC70	Analogue to digital converter
&FC71	Parallel printer port
&FC72	Status register
&FC73	ROM scrolling register
&FC78 to &FC7F	Laser Disc
&FC80 to &FC8F	Test Hardware
&FC90 to &FC9F	Sound/Speech
&FCB0 to &FCBF	VIA
&FCC0 to &FCCF	Floppy Disc Controller
&FCE0 to &FCEF	Tube
&FCFF	Paged RAM register