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Support Group Application Note
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Author:

1MHz Bus Application Note

Applicable Hardware :

BBC B
BBC B+
BBC Master 128

Related Application Notes:

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Cambridge CB4 4AE

CONTENTS

DRAWINGS

1 INTRODUCTION

The BBC Microcomputer has been designed to allow expansion in a number of ways. In addition to the specialised Disc and Printer plugs, there are three "general" expansion facilities. For these facilities, the Model B has IDC headers mounted at the front edge of the main board, accessed from the underside of the case.

The Tube interface and the user port will be discussed in other application notes. This note describesd the signal available on the 1Megahertz Bus, the circuitry required to utilise them, and the way in which they are connected to the Acorn Expansion Box. The expansion memory map is also defined. When interfacing designs to the 1MHz Bus, it is vital to ensure compatability with Acorn standards, to prevent problems when using several peices of equipment on the bus simultaneously.

Remember that the standards cover both hardware and software protocols.

It is as important for the software to follow these guidelines as it is for the hardware, otherwise simultaneous operations of several peripherals may not be possible.

The standards described allow up to 64K of pages address space to be accessed as well as 255 bytes of direct access ports.

2 SIGNAL DEFINITIONS

The following lines are available on the 1MHz Expansion Connector:

A0 - A7 (pins 27-34)	The low eight address lines from the 6502, buffered by a 74LS244 (IC 71) permanently enabled.
D0 - D7 (pins 18-25)	A bi-directional data bus connected to the CPU through IC 72, a 74LS245 buffer. The direction of data is determined by the system Read-not-write (R/W) line. The buffer is only enabled if NPGFC or NPGFD is low (see below).
Analogue In (pin 16)	An input to the BBC Microcomputer audio circuitry. Input impedance is 9K ohms. A siganl of +/-3 volts RMS will produce a saturated siganl at the loudspeaker (full volume), though signals this large will cause distortion if the on-board sound or speech is used at the same time.
NRST (pin 14)	Not Reset. This is an OUTPUT ONLY for the system reset line (active low). It may be used to initialise peripherals on power-up and when the "BREAK" key is pressed.
NPGFC & NPGFD (pins 10 & 12)	"Not page FC" and "Not page FD". Page select signals decoded from the top eight address bits of the system data bus. These signals are active low. Pages FC and FD (ie FC00 to FCFF and FD00 to FDFF hex) are the only pages available for general expansion. However, the paging register described in Section 5 allows a much larger address space to be accessed.

NIRQ (pin 8)	Not Interrupt Request (active low). The system IRQ line which is open collector (ie "wired-or") and may be asserted by devices attached to the extension bus. The pull-up resistor on this line is 3K3. IRQ is level triggered and it is absolutely essential for correct operation of the machine that interrupts do not occur until the software is capable of dealing with them. Interrupts on the 1MHz bux should therefore be disabled on power-up and reset conditions. Significant use of interrupt service time may affect other machine functions. In particular, masking interrupts for more than 10mS will affect the real time clock.
NNMI (pin 6)	Not Non-Maskable Interrupt (active low). The system NMI line which is open collector (ie wired-or) and may be asserted by devices attached to the extension bus. The pull-up resistor on this line is also 3K3. It should be remembered that NMI is nagative edge triggered and that both the disc and net chips on the main board use this line. Caution must be exercised to avoid masking other interrupts by holding the line low. Use of NMI facilities on the BBC machine requires an advanced knowledge of 6502 programming techniques and the Operating System protocols.
IMHzE (pin 4)	A system clock timing signal which is a 1MHz 50% duty-cycle square wave. During access to 1MHz peripherals and to the extension bux the processor clock (normally 2MHz) is streched so that the trailing edges of 1MHzE and processor clock are coincident.
R/W (pin 2)	The system Read Not Write signal which is derived from the CPU R/W siganl through two 74LS04 inverters.
0V (pins 1,3,5,7,9,11,13,15,17,26)	System 0V, ie GND wires, dispersed so as to interleave with] asynchronous groups of signals in a flat ribbon cable.

3 HARDWARE REQUIREMENTS FOR 1MHZ EXPANSION BUS PERIPHERALS

1 No power may be drawn from the BBC Microcomputer. Easch peripheral should have its own integral power supply, although a separate power unit may be used.

2 Not more than one low-power Schottky TTL load may be presented to any bus line by each peripheral.

3 A 1MHz bus feed-through connector should be provided. Connection to the BBC Microcomputer should be via 600mm of 34-way ribbon cable terminated with a 34-way IDC socket, and fitted with strain relief. Please note that copying the Teletext Adapter's layout is not possible, because this has been given the special status of the last box in the chain.

4 Opetional bus termination should be provided on all bus lines except NRST, NNMI and NIRQ. the recommended termination is a 2K2 resistor to +5V and a 2K2 resistor to ground for each line.

5 The timing requirements for the 1MHz bus are detailed in Figure 1.

4 FURTHER REQUIREMENTS FOR EQUIPMENT TO BE APPROVED BY ACORN COMPUTERS

1 Address space within page &FC must be allocated by the Research and Development Department of Acorn Computers Ltd - see Section 6.

2 The dimensions of any peripheral and its associated integral power supplies should allow it to be fitted into the BBC Microcomputer Expansion Box - see Figure 4.

3 When housed in the Expansion Box, the equipment should meet BS415 Class 1 specifications for Electrical safety.

Further details of the requirements and procedures for gaining approval should be obtained from Acorn. The information included here is for guidance only and is not intended to be a full specification for approval.

5 DERIVATION OF VALID PAGE SIGNALS

1MHz peripherals are clocked by a 1MHz 50% duty cycle square wave (chosen to allow chips such as the 6522 to use their timing elements reliably). The BBC Microcomputer's cpu normally operates with a 2MHz clock, but with a slow-down circuit which has the effect of stretching the "clock high" period immediately following the detection of a valid 1MHz peripheral address.

There are two problems as a result of this. First, addresses will change and may momentarily become 1MHz addresses while the 2MHz cpu clock is low, but while the 1MHzE signal is high. this could give rise to a spurious pulse on the chip select. Second, if the cpu deliverately addresses a 1MHz peripheral during the time that 1MHzE is high, the device will be addressed immediately, and then again when 1MHzE is next high: this is because the cpu clock will be held "high" by the stretching ciruit until the next coincident falling edge of the 1MHz and 2MHz clocks. See Figure 2: the two accesses are marked C and D. this double access is not usually a problem except when reading from or writing to a location twice has some additional effect: an example of this is an interrupt flag which is cleared by reading it.

These effects mean that the 1MHzE bux cannot be used a a conventional "address valid" signal. However, addresses will always be valid on the rising edgte of 1MHzE. If the chip select lines are latched by 1MHzE as shown in Figure 2, the clean signal CNGFC (or CNPGFD) will be generated.

6 ADDRESS SPACE ALLOCATION

PAGE FC

Page FC is reserved for peripherals with small memory requirements. Only one peripheral will be allocated to each group of addresses. Further allocations must be agreed with the R & D Department of Acorn Computers Ltd.

Initial allocations are:

FC00 to FC0F	Test Hardware
FC10 to FC13	Teletext
FC14 to FC1F	Prestel
FC20 to FC27	IEEE 488 Interface
FC28 to FC2F	Acorn Expansion: Spare
FC30 to FC3F	Cambridge Ring Interface
FC40 to FC47	Winchester Disc Interface
FC48 to FC7F	Acorn Expansion: Spare
FC80 to FC8F	Test Hardware
FC90 to FCBF	Acorn Expansion: Spare
FCC0 to FCFE	User Applications
FCFF	Paging Register

PAGE FD

Page FD is used in conjunction with the paging regisger to provide a 64K address space, accessed one page at a time. Each BBC Expansion Box will have a paging register on the backplane, thus data will be latched simultaneously on every Expansion Box. Data latched into the paging register will provide the top eight address bits to the eurocard backplane. These top address bits are referred to as the 'Extended Page Number'. Any peripheral designed to locate in page RD without using an expansion backplane must latch and decode the paging address inforation.

To make this facility as easy to use as possible, NPGFD (a hazard free version of the signal available from PL 12) will be connected to the backplane pin 24b, 'Not Valid memory Address', and also OR-ed with the top four extended page address lines as a link selectable option to pin 31a 'BLKO'. (The other option on this pin will be NPGFC).

Extended pages &00 to &7F are reserved for Acorn use, pages &80 to &FF may be freely used by special applicatons. The paging register will be reset to &00 on power-up and BREAK.

Since the paging register is a write-only latch, location &00EE in the zero page of the BBC machine addressmap has been allocated as a RAM image of the register. Note that this location will remain in the I/O processor's memory map if a second processor is fitted.

The importance of this image is that it allows interrupt routines to change the paging register and restore it again afterwards.

It is vital to change location &00Ee BEFORE changing the paging register itself. It you do not, then an interrupt may occur before you change the RAM image and this will restore the paging register to the old value of &EE.

A suitable sequence is:

```
LDA  #  new value
STA  &EE
STA  &FCFF                    MACHINE CODE

          OR. . . . .

?&EE  =  new value
?&FCFF  = new value           BASIC
```

User routines should save the contents of &EE beforfe changing the paging register and restore both &Ee and &FCFF to this value before returning from the interrupt.

A suitable sequence is:

```
[save processor registers etc.]

LDA  &EE
STA  tempstore
LDA  #  new value
STA  &EE
STA  &FCFF

[users code here]

STA  &EE
STA  &FCFF

[restore other data and return]
```

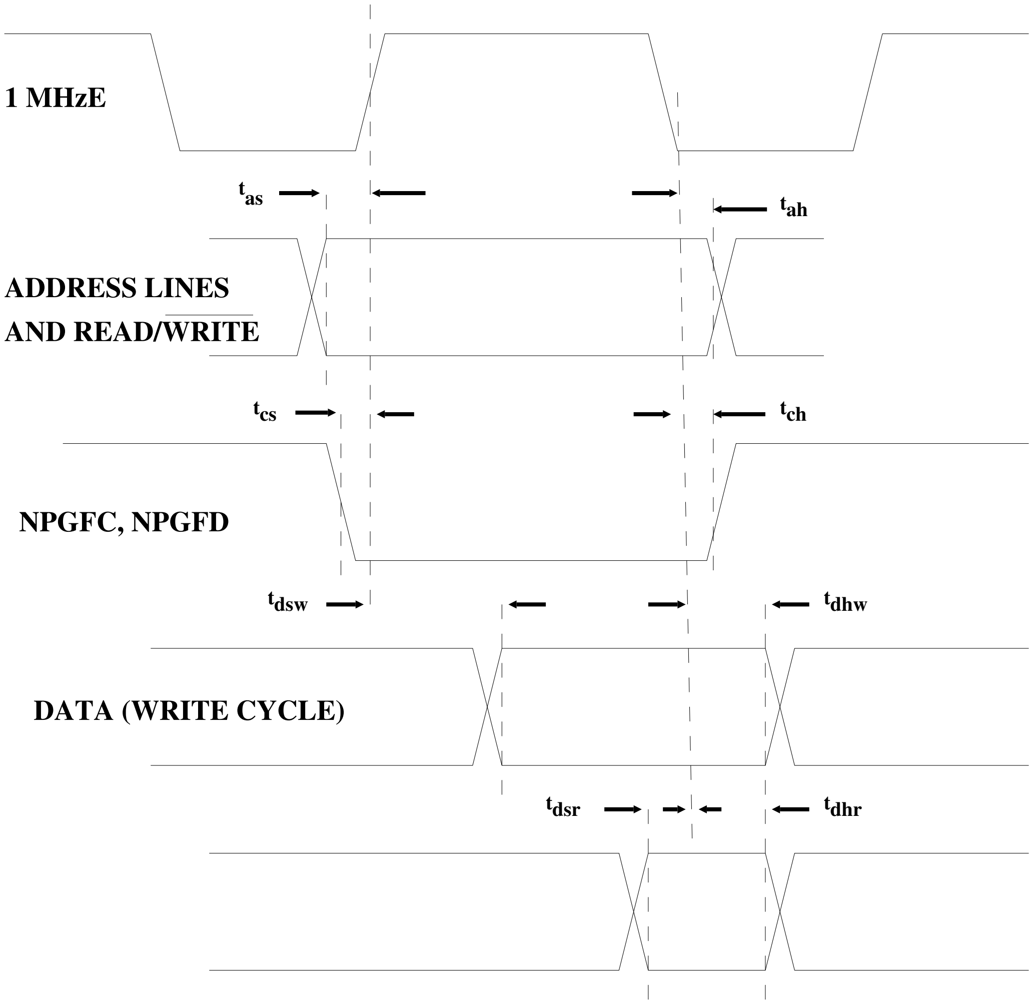

FIGURE 1 : 1MHz BUS TIMING DIAGRAM

Timing requirements

Parameter	Symbol	Min	Max
Address Set-up Time (&R/W Set-up Time)	t as	300	1000
Address Hold Time (&R/W Hold Time)	t ah	30	-
NPGFC & NPGFD Set-up Time	t cs	250	1000
NPGFC & NPGFD Hold Time	t ch	30	-
Write Data Set-up Time	t dsw	-	150
Write Data Hold Time	t dhw	50	-
Read Data Set-up Time	t dsr	200	-
Read Data Hold Time	t dhr	30	-

Note: The above timings are based on only one peripheral attached to the Expansion Bus. Heavy loading may slow the rise and fall times of 1MHzE with possible adverse effects on timings.

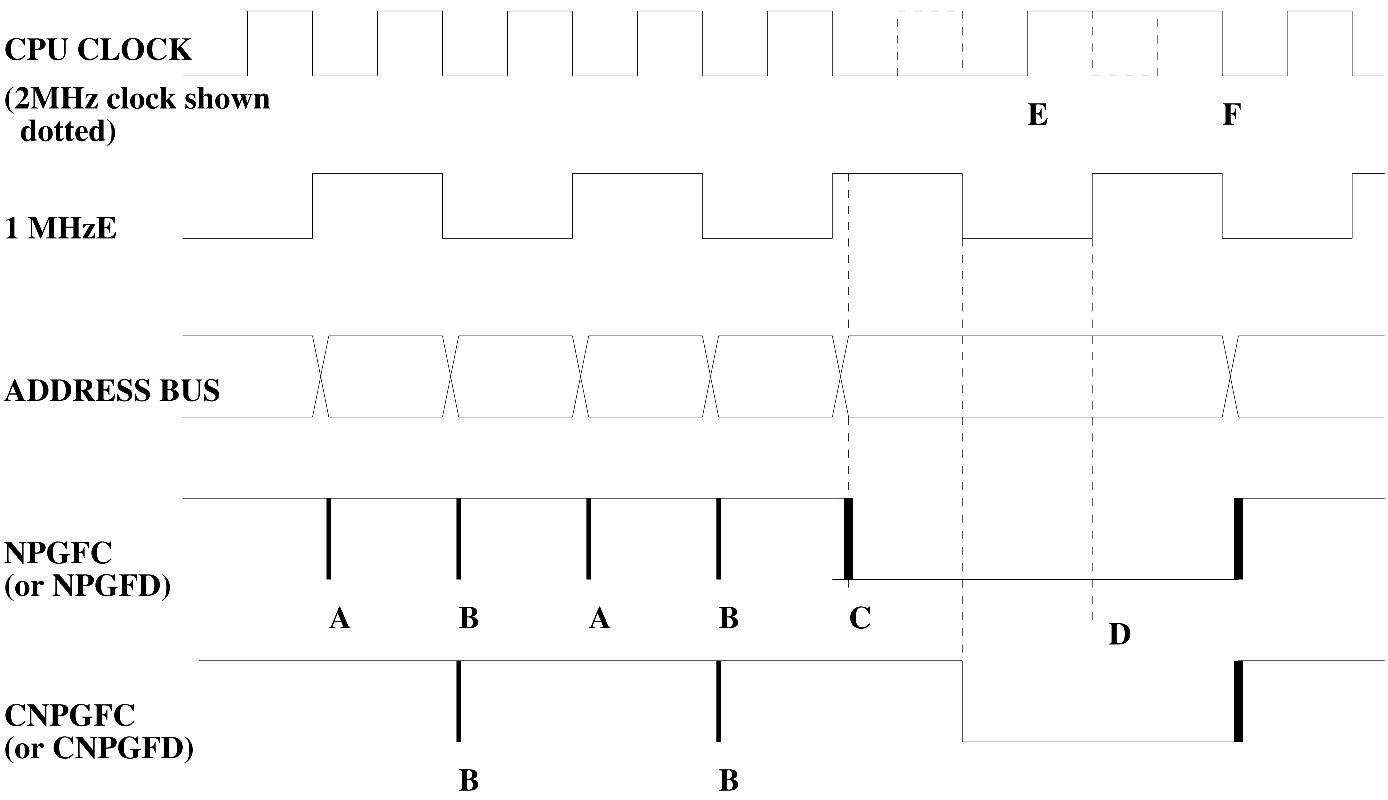

FIGURE 2 : DERIVATION OF VALID PAGE SELECT SIGNAL

As the address lines settle, a momentary pulse could occur on the NPGFC (or NPGFD) line. The pulses at B are ignored because 1MHzE is low, but those at A could cause a spurious access.

When a valid 1MHz device address appears, NPGFC (or NPGFD) goes low: this can happen as shown whilst 1MHzE goes high, accessing the device. when a 1MHz address is detected, the clock stretching circuit waits if necessary for the next rising edge of the 2MHz clock (point E), and holds the cpu clock (point F). Hence the device is accessed again at point D, when 1MHzE is next high. The gated signal CNPGFC (or CNPGFD) removes the glitches A and the first of the two accesses at C.

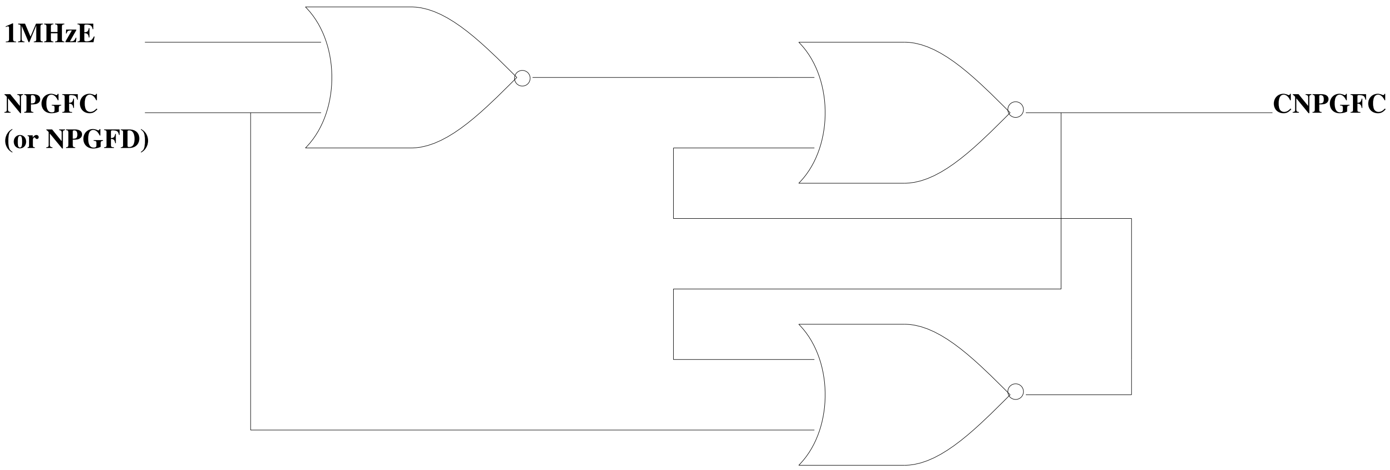

FIGURE 3 : DERIVATION OF CLEAN SELECT SIGNALS

R-S flip-flop with gated input which allows 'clean select' to be set low only if 1MHzE is low. An alternative circuit using transparent flip-flops is shown on the circuit diagram for the Expansion box backplane (Drawing 107,000).

NOTE: All dimensions in millimetres

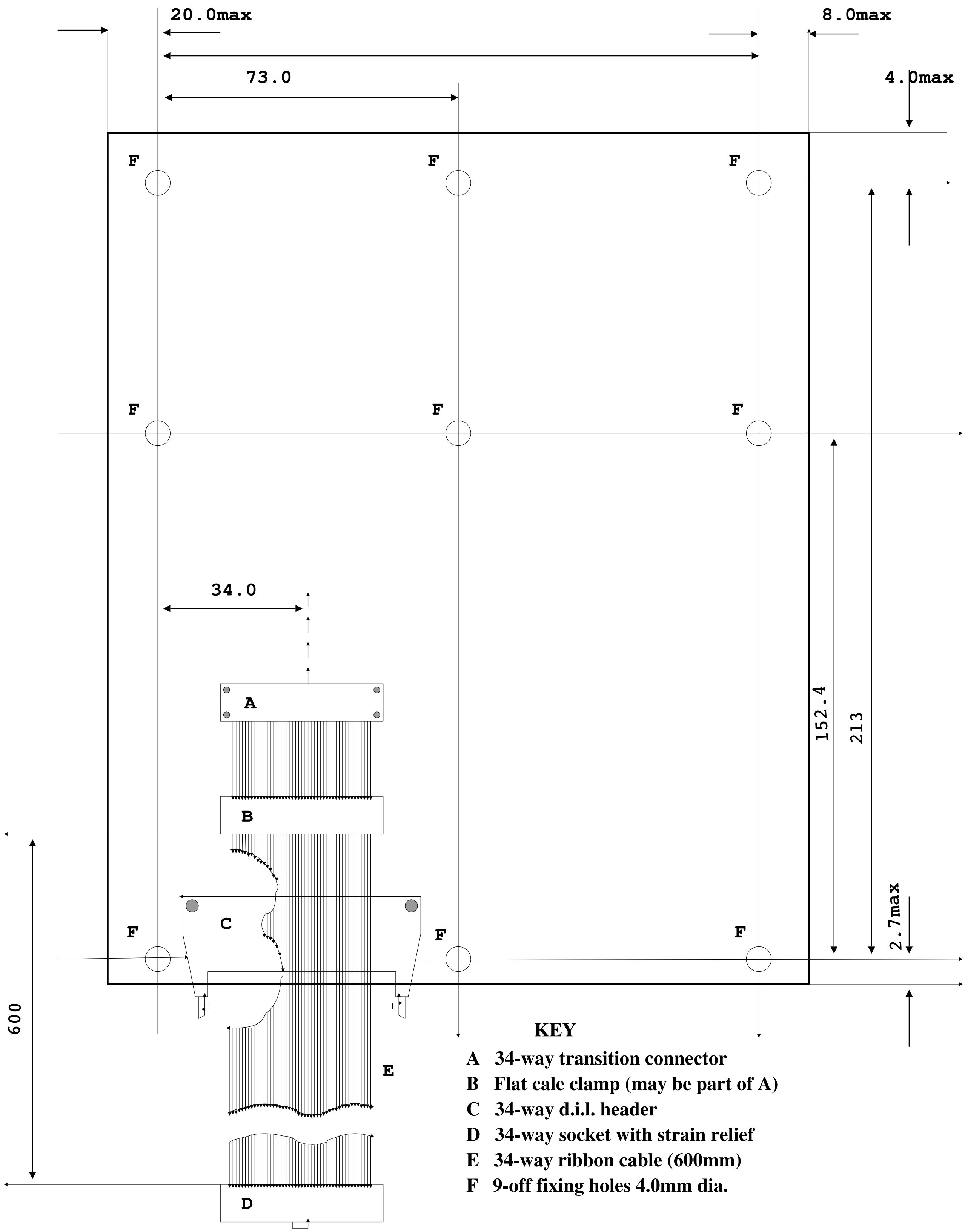

FIGURE 4 : BOARD DIMENSIONS TO FIT BBC MICROCOMPUTER EXPANSION BOX